RAMAIAH
Institute of Technology

CURRICULUM

Academic year 2022 – 2023

ELECTRONICS AND COMMUNICATION ENGINEERING

V & VI SEMESTER B.E.

RAMAIAH INSTITUTE OF TECHNOLOGY
(Autonomous Institute, Affiliated to VTU)
Bangalore – 560054.

About the Institute:

Dr. M. S. Ramaiah a philanthropist, founded 'Gokula Education Foundation' in 1962 with an objective of serving the society. M S Ramaiah Institute of Technology (MSRIT) was established under the aegis of this foundation in the same year, creating a landmark in technical education in India. MSRIT offers 17 UG programs and 15 PG programs. All these programs are approved by AICTE. All eligible UG and PG programs are accredited by National Board of Accreditation (NBA). The institute is accredited with **'A^{+}' grade by NAAC in March 2021** for 5 years. University Grants Commission (UGC) & Visvesvaraya Technological University (VTU) have conferred Autonomous Status to MSRIT for both UG and PG Programs since 2007. The institute is also been conferred autonomous status for Ph.D program since 2021. The institute is a participant to the Technical Education Quality Improvement Program (TEQIP), an initiative of the Government of India. The institute has 380 competent faculty out of which 65% are doctorates. Some of the distinguished features of MSRIT are: State of the art laboratories, individual computing facility for all faculty members, all research departments active with sponsored funded projects and more than 300 scholars pursuing Ph.D. To promote research culture, the institute has established Centre of Excellence for Imaging Technologies, Centre for Advanced Materials Technology, Centre for Antennas and Radio Frequency systems (CARFS), Center for Cyber Physical Systems, Schneider Centre of Excellence & Centre for Bio and Energy Materials Innovation. **M S Ramaiah Institute of Technology has obtained "Scimago Institutions Rankings" All India Rank 107 & world ranking 600 for the year 2022.** The Entrepreneurship Development Cell (EDC) and Section 8 company "Ramaiah Evolute" have been set up on campus to incubate startups. **M S Ramaiah Institute of Technology is recognized by Atal Ranking of Institutions on Innovation Achievements (ARIIA), MoE, Govt. of India.** MSRIT has a strong Placement and Training department with a committed team, a good Mentoring/Proctorial system, a fully equipped Sports department, large air-conditioned library with good collection of book volumes and subscription to International and National Journals. The Digital Library subscribes to online e-journals from Elsevier Science Direct, IEEE, Taylor & Francis, Springer Link, etc. MSRIT is a member of DELNET, CMTI and VTU E-Library Consortium. MSRIT has a modern auditorium and several hi-tech conference halls with video conferencing facilities. The institute has excellent hostel facilities for boys and girls. MSRIT Alumni have distinguished themselves by occupying high positions in India and abroad and are in touch with the institute through an active Alumni Association.

As per the National Institutional Ranking Framework (NIRF), MoE, Government of India, M S Ramaiah Institute of Technology has achieved 67th rank among 1249 top Engineering Institutions & 17th Rank for School of Architecture in India for the year 2022 and is 1st amongst the Engineering Colleges affiliated to VTU, Karnataka.

About the Department

The Department of Electronics and Communication was started in 1975 and has grown over the years in terms of stature and infrastructure. The department has well equipped simulation and electronic laboratories and is recognized as a research center under VTU. The department currently offers a B. E. program with an intake of 120, and two M. Tech programs, one in Digital Electronics and Communication, and one in VLSI Design and Embedded Systems, with intakes of 30 and 18 respectively. The department has a Center of Excellence in Food Technologies sponsored by VGST, Government of Karnataka. The department is equipped with numerous UG and PG labs, along with R & D facilities. Past and current research sponsoring agencies include DST, VTU, VGST and AICTE with funding amount worth Rs. 1 crore. The department has modern research ambitions to develop innovative solutions and products and to pursue various research activities focused towards national development in various advanced fields such as Signal Processing, Embedded Systems, Cognitive Sensors and RF Technology, Software Development and Mobile Technology.

Vision of the Institute

To be an Institution of International Eminence, renowned for imparting quality technical education, cutting edge research and innovation to meet global socio-economic needs

Mission of the Institute

RIT shall meet the global socio-economic needs through

- *Imparting quality technical education by nurturing a conducive learning environment through continuous improvement and customization*
- *Establishing research clusters in emerging areas in collaboration with globally reputed organizations*
- *Establishing innovative skills development, techno-entrepreneurial activities and consultancy for socio-economic needs*

Quality Policy

We at M. S. Ramaiah Institute of Technology strive to deliver comprehensive, continually enhanced, global quality technical and management education through an established Quality Management System complemented by the synergistic interaction of the stake holders concerned

Vision of the Department

To evolve into a department of national and international repute for excellence in education and cutting-edge research in the domain of Electronics and Communication Engineering

Mission of the Department

The department will continuously strive to

1. *Provide a world-class learning environment that caters to local and global technological and social requirements*
2. *Initiate research collaborations with academia and industries to perform cutting edge research leading to socio-technological innovations*
3. *Develop skills for pursuing innovation and entrepreneurial ventures for graduating engineers*

Program Educational Objectives (PEOs):

PEO1: *Acquire knowledge and skills to be employed as successful professionals in their chosen careers*

PEO2: *Emerge as technologists, researchers, and entrepreneurs through lifelong learning*

PEO3: *Demonstrate social, ethical, and leadership skills*

Program Outcomes (POs):

PO1: ***Engineering Knowledge:*** *Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.*

PO2: ***Problem Analysis:*** *Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.*

PO3: ***Design/development of Solutions:*** *Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.*

PO4: ***Conduct Investigations of Complex Problems:*** *Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions*.

PO5: ***Modern Tool Usage:*** *Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.*

PO6: ***The Engineer and Society:*** *Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.*

PO7: ***Environment and Sustainability:*** *Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.*

PO8: ***Ethics:*** *Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.*

PO9: ***Individual and Teamwork:*** *Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.*

PO10: ***Communication:*** *Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.*

PO11: ***Project Management and Finance:*** *Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.*

PO12: ***Life-long Learning:*** *Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.*

Program Specific Outcomes (PSOs):

PSO1: ***Circuit Design Concepts:*** *Apply basic and advanced electronics for implementing and evaluating various circuit configurations.*

PSO2: ***VLSI and Embedded Domain:*** *Demonstrate technical competency in the design and analysis of components in VLSI and embedded domains.*

PSO3: ***Communication Theory and Practice:*** *Possess application level knowledge in theoretical and practical aspects required for the realization of complex communication system*

Distribution of credits for the batch of 2019 – 2023

Course Category	1st	2nd	3rd	4th	5th	6th	7th	8th	Total
Basic Science (BSC)	9	8	4	4					25
Engineering Science (ESC)	11	10							21
Humanities and Management (HSMC)		2			3		3		08
Professional Courses – Core (PCC)			21	21	15	11	10		78
Professional Courses – Elective (PCE)					3	6	6		15
Open Elective (OE)					3	3			06
Project Work (PW)						4	1	17	22
Total	20	20	25	25	24	24	20	17	175

SCHEME OF TEACHING (2021 – 2022)

V SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	EC51	Communication Systems	PCC	3	1	0	4	5
2.	EC52	CMOS VLSI Design	PCC	4	0	0	4	4
3.	EC53	Microwave Devices & Antennas	BSC	3	1	0	4	5
4.	EC54	Entrepreneurship & Management	HSMC	3	0	0	3	3
5.	ECE55x	Professional Elective – I	PCE	3	0	0	3	3
6.	XXOExx	Open Elective – I	OE	3	0	0	3	3
7.	ECL56	Communication Systems Laboratory – I	PCC	0	0	1	1	2
8.	ECL57	CMOS VLSI Laboratory	PCC	0	0	1	1	2
9.	ECL58	Microwave & Antennas Laboratory	PCC	0	0	1	1	2
			Total	**19**	**2**	**3**	**24**	**29**

VI SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	EC61	Analog & Mixed Signal VLSI Design	PCC	3	1	0	4	5
2.	EC62	Embedded System Design	PCC	3	1	0	4	5
3.	ECE63x	Professional Elective – II	PCE	3	0	0	3	3
4.	ECE64x	Professional Elective – III	PCE	3	0	0	3	3
5.	XXOExx	Open Elective – II	OEC	3	0	0	3	3
6.	EC65	Mini Project/Professional Elective/NPTEL Course	PW/PCE	0	0	4	4	8
7.	ECL66	Communication Systems Laboratory – II	PCC	0	0	1	1	2
8.	ECL67	Analog &Mixed Signal VLSI Laboratory	PCC	0	0	1	1	2
9.	ECL68	Embedded System Design Laboratory	PCC	0	0	1	1	2
			Total	**15**	**2**	**7**	**24**	**33**

LIST OF DEPARTMENT ELECTIVES

Sl. No.	Course Code	Course Title	Credits			
			L	T	P	Total
V Semester (Elective I)						
1.	ECE551	Information, Learning and Inference	3	0	0	3
2.	ECE552	Advanced Digital Design	3	0	0	3
3.	ECE553	Operating Systems	3	0	0	3
4.	ECE554	Computer Architecture	3	0	0	3
VI Semester (Elective II)						
5.	ECE631	Image and Video Processing	3	0	0	3
6.	ECE632	Advanced Digital Logic Verification	3	0	0	3
7.	ECE633	Error Control Coding	3	0	0	3
8.	ECE634	Robotics	3	0	0	3
VI Semester (Elective III)						
9.	ECE641	Radars and Satellite Communication	3	0	0	3
10.	ECE642	Machine and Deep Learning	3	0	0	3
11.	ECE643	Speech and Audio Processing	3	0	0	3
12.	ECE644	Low Power VLSI Design	3	0	0	3
VII Semester (Elective IV)						
13.	ECE741	Automotive Electronics	3	0	0	3
14.	ECE742	MEMS And Nanoelectronics	3	0	0	3
15.	ECE743	Computer Vision	3	0	0	3
16.	ECE744	Optical Fiber Communication	3	0	0	3
VII Semester (Elective V)						
17.	ECE751	Modeling and Simulation	3	0	0	3
18.	ECE752	Cryptography, Network and Cyber Security	3	0	0	3
19.	ECE753	Multimedia Communication	3	0	0	3
20.	ECE754	Advanced Embedded Systems	3	0	0	3

LIST OF OPEN ELECTIVES OFFERED FROM THE DEPARTMENT

Sl. No.	Course Code	Course Title	Credits			
			L	T	P	Total
1.	ECOE01	Microcontroller and Applications	3	0	0	3
2.	ECOE02	Image Processing with Python	3	0	0	3
3.	ECOE03	Fundamentals of Neural Networks	3	0	0	3
4.	ECOE04	Sensor Electronics	3	0	0	3
5.	ECOE05	Automotive Electronics	3	0	0	3
6.	ECOE06	Embedded and Internet of Things	3	0	0	3

COMMUNICATION SYSTEMS

Course Code: EC51 **Credits: 3:1:0**
Prerequisites: Linear Integrated Circuits, Signal and Systems **Contact Hours: 70**
Course Coordinator: T. D. Senthilkumar

UNIT – I

Amplitude Modulation: Introduction to AM: Time domain description, Frequency domain description. Generation of AM wave: Square law modulator, switching modulator. Detection of AM waves: Square law detector, envelope detector, time domain description of DSBSC, Frequency domain representation, Generation of DSBSC waves, ring modulator, coherent detection of DSBSC modulated waves

UNIT – II

Angle Modulation (FM): Generation of FM waves: indirect FM and direct FM, frequency discrimination method, phase locked loop, non-linear model of phase locked loop, linear model of phase locked loop

Noise in Continuous Wave Modulation Systems: Receiver model, noise in AM receivers, noise in FM receivers, pre-emphasis and de-emphasis in FM

UNIT – III

Signal Sampling: Basic signal processing operations in digital communication, sampling principles, Sampling Theorem, Practical aspects of sampling and signal recovery, PAM, TDM

Waveform Coding Techniques: PCM block diagram, Different quantization techniques, SNR in PCM Robust quantization, DPCM, DM

UNIT – IV

Base Band Shaping for Data Transmission: Line Codes and their power spectra

Inter Symbol Interference: Introduction, Nyquist criterion for distortion less base-band binary transmission, correlative coding, duo binary coding, Eye pattern

Detection: Model of digital communication system, Gram – Schmidt orthogonalization, geometric interpretation of signals, Maximum likelihood detection

UNIT – V

Detection: Correlation receiver, Matched Filter Receiver, Properties of Matched Filter

Digital Modulation and Demodulation Techniques: Binary modulation techniques, BPSK, FSK, ASK, QPSK and DPSK systems with signal space diagram, generation, demodulation and error probability

Text Books:

1. Simon Haykin, Michael Moher, "Introduction to Analog and Digital Communication", 2nd Edition, Wiley India Pvt. Ltd., 2012.
2. H. Taub, D. L. Schilling, "Principles of Communication Systems", 2nd Edition, McGraw Hill, Reprint, 2008.

References:

1. Bernard Sklar, "Digital Communications", 2nd Edition, Pearson Education, 2007.
2. B. P. Lathi and Zhi Ding, "Modern Digital and Analog Communication Systems", 4th International Edition, Oxford University Press, 2015.
3. George Kennedy, Bernard Davis, S R M Prasanna, "Electronic Communication Systems", 5th Edition, McGraw-Hill, 2011.

Course Outcomes (COs):

1. Analyze the generation and demodulation of AM and DSBSC systems. (POs – 1, 2, 3, 4, 8,12, PSOs – 1, 3)
2. Discuss FM generation and analyze its performance in the presence of noise. (POs – 1, 2, 3, 4, 8,12, PSOs – 1, 3)
3. Analyze the performance of the different waveform coding techniques. (POs – 1, 2, 3, 4, 8,12, PSO – 3)
4. Discuss encoding of base band signal, pulse shaping filter design and maximum likelihood estimation. (POs – 1, 2, 3, 4, 8,12, PSO – 3)
5. Interpret the signal space concepts in generation and detection of different digital modulation techniques. (POs – 1, 2, 3, 4, 8,12, PSO – 3)

CMOS VLSI DESIGN

Course Code: EC52 **Credits: 4:0:0**
Prerequisites: Digital Design **Contact Hours: 56**
Course Coordinator: Raghuram S

UNIT – I

Introduction to VLSI Design: Structured Design Strategies, Design Methods, Design Flows, Logic and Circuit Design, Physical Design, Design Verification, Fabrication, Packaging and Testing, Scaling: Moore's Law, Dennard's Law

CMOS Processing Technology: Fabrication Process, CMOS Technologies, Layout Design Rules, CMOS Process Enhancements, SoI and FinFETs

UNIT – II

MOS Transistor Theory: Long Channel V-I Characteristics, C-V Characteristics, Non-ideal V-I Characteristics, DC Transfer Characteristics

CMOS Logic Circuits: The Inverter, CMOS Gates, Compound Gates, Pass Transistor Gates, Tri-States, MUXes, Stick Diagram, Layouts, Sequential Circuits

UNIT – III

Datapath Subsystems: Adders: Ripple carry, Carry generate and propagate, Propagate Generate Logic, Manchester Carry Chain, Carry select, Carry look ahead, Tree Adders, Subtraction, Multiple input addition, Multiplication: Unsigned Array Multiplication, Two's Complement Array Multiplication, Booth Encoding

UNIT – IV

Delay: Transient Response, Delay Estimation: Effective Resistance and Capacitance, RC Delay Model, Elmore Delay Model, Linear Delay Model, Logical Effort (LE), Method of LE and transistor sizing: Delay in gates and multistage networks, Choosing the best number of stages with the method of LE

UNIT – V

Combinational Circuit Design: Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass-Transistor Circuits, SoI Circuit Design, Sub-threshold circuit design

Sequencing Static Circuits: Sequencing Methods, Max-Delay and Min-Delay Constraints, Time Borrowing, Clock Skew

Text Books:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuit and Systems Perspective", 4th Edition, Pearson Education, 2015.

References:

1. Jan Rabaey, B.Nikolic, A.Chandrakasan, "Digital Integrated Circuits: A Design Perspective", 2nd Edition, Pearson, 2003.
2. Morris Mano, Michael Ciletti, "Digital Design", 5th Edition, Pearson Education, 2013.

Course Outcomes (COs):

1. Discuss the aspects of the VLSI design flow the steps in the CMOS fabrication technology (POs – 1, 2, 3, 4, 5,8, 9, 10, 11,12, PSO – 2)
2. Predict the performance of a MOS transistor, and apply its functionality to design digital circuits (POs —1, 2, 3, 4, 5,8, 9, 10, 11,12, PSO – 2)
3. Describe various connection configurations to realize datapath elements and analyze their operating speed (POs —1, 2, 3, 4, 5,8, 9, 10, 11,12, PSO – 2)
4. Evaluate the delay due to a MOS logic circuit, and thereby design a circuit to satisfy design parameters (POs —1, 2, 3, 4, 5,8, 9, 10, 11,12, PSO – 2)
5. Analyze the performance of various MOS circuit families and discuss timing constraints of sequential digital circuits (POs – 1, 2, 3, 4, 5,8, 9, 10, 11,12, PSO – 2)

MICROWAVES AND ANTENNAS

Course Code: EC53 **Credits: 3:1:0**
Prerequisites: Field, Lines and Waves **Contact Hours: 70**
Course Coordinator: Sujatha B.

UNIT – I

Multiport Microwave Network Analysis: Impedance, admittance and transmission matrices of reciprocal microwave networks and lossless microwave networks, Scattering matrix – reciprocal networks and lossless networks, shift in reference planes, Basic properties of dividers and couplers – three-port networks, four-port networks; T-junction power divider – lossless divider, resistive divider, Wilkinson power divider – even-odd mode analysis

UNIT – II

Microwave Devices and Tubes: PIN diodes, Schottky-barrier diode, Attenuator, RWH theory, Gunn diodes– Gunn Effect, modes of operation. Two cavity klystron amplifiers, Reflex Klystrons: Mathematical analysis of power and efficiency, Traveling Wave Tubes, Magnetron Oscillators.

UNIT – III

Fundamentals of Antennas: Principle of antenna, fields from oscillating dipole, antenna field zones, basic antenna parameters, patterns, beam area, Radiation intensity, beam efficiency, directivity and gain, antenna aperture, effective height and radio communication link (Friis formula).

UNIT – IV

Point Source and Arrays: Point source, Types of Arrays (Broad side, End fire, Extended End fire), Arrays of two point sources, linear array of n-isotropic point sources of equal amplitude and spacing, null direction for arrays n isotropic point source of equal amplitude and spacing, pattern multiplication.

UNIT – V

Types of Antennas: Introduction, Thin linear antenna, field components of $\lambda/2$ (hertz) dipole antenna, Radiation resistance of dipole antenna. Directivity of dipole antenna, Yagi-Uda antenna, Horn antenna, parabolic reflectors, Micro strip rectangular patch antenna design.

Text Books:

1. David M. Pozar, "Microwave Engineering", 4th Edition, Wiley Publications, 2011.
2. Samuel Y Liao, "Microwave Devices and Circuits", 3rd Edition, Pearson Education, 2011.
3. John D Kraus, Ronald J Marhetka, Ahmad S Khan, "Antennas and Wave Propagation", 5th Edition, Tata McGraw Hill, 2017.

References:

1. Annapurna Das, Sisir K Das, "Microwave Engineering", 3rd Edition, McGraw-Hill, 2015.
2. Constantine A Balanis, "Antenna, Theory, Analysis & Design", 4th Edition, John Wiley & Sons, 2016.

Course Outcomes (COs):

1. Apply the properties of scattering parameters to obtain the S-matrix of microwave components and circuits (POs – 1, 2, 3, 8, 10, 12, PSOs –1, 3)
2. Illustrate the significance of various microwave passive devices and tubes (POs – 1, 2, 3, 8, 10, 12, PSOs –1, 3)
3. Describe the parameters of antennas (POs – 1, 2, 3, 8, 10, 12, PSOs –1, 3)
4. Design different types of arrays and study the concept of pattern multiplication (POs – 1, 2, 3, 8, 10, PSOs –1, 3)
5. Explore the field components and radiation resistance of various antennas (POs – 1, 2, 3, 8, 10, PSOs –1, 3)

ENTREPRENEURSHIP AND MANAGEMENT

Course Code: EC54 **Credits: 3:0:0**
Prerequisites: -- **Contact Hours: 42**
Course Coordinator: V. Nuthan Prasad

UNIT – I

Management: Management Functions, Roles of Manager, Levels of Management, Managerial Skills, Management & Administration, Management as a Science, Art & Profession Planning: Nature, Importance and Purpose of Planning, Types of Plans, Steps in Planning, Limitations of Planning, Decision Making – Meaning, Types of Decisions Steps in Decision Making

Standard Management Practices: Performance Monitoring, Target Setting, Incentive Setting

Introduction to Standards: ISO, CMMI

UNIT – II

Organizing: Meaning, Nature and Characteristics of Organization – Process of Organization, Principles of Organization, Departmentalization, Committees – meaning, Types of Committees, Centralization Vs Decentralization of Authority and Responsibility, Span of Control (Definition only)

Directing and Controlling: Meaning and Nature of Directing – Leadership Styles, Motivation Theories Communication – Meaning and Importance, Coordination – Meaning and Importance, Techniques of Coordination. Controlling – Meaning, Steps in Controlling

Human Resource Management: Nature and Importance of Staffing, Process of Selection and Recruitment, Performance Management, Compensation and Benefits.

UNIT – III

Social Responsibilities of Business: Meaning of Social Responsibility, Social Responsibilities of Business towards Different Groups, Social Audit, Business Ethics and Corporate Governance

Entrepreneurship: Definition of Entrepreneur, Importance of Entrepreneurship, concepts of Entrepreneurship, Characteristics of successful Entrepreneur, Classification of Entrepreneurs, Intrepreneur – An Emerging Class, Comparison between Entrepreneur and Intrepreneur, Myths of Entrepreneurship, Entrepreneurial Development models, Entrepreneurial development cycle, Problems faced by Entrepreneurs and capacity building for Entrepreneurship

UNIT – IV

Modern Small Business Enterprises: Role of Small Scale Industries, Concepts and definitions of SSI Enterprises, Government policy and development of the Small Scale sector in India, Growth and Performance of Small Scale Industries in India, Sickness in SSI sector, Problems for Small Scale Industries, Impact of Globalization on SSI, Impact of WTO/GATT on SSIs, Ancillary Industry and Tiny Industry (Definition only). Institutional Support for Business Enterprises: Introduction, Policies & Schemes of Central–Level Institutions, State-Level Institutions

UNIT – V

Project Management: Meaning of Project, Project Objectives & Characteristics, Project Identification-Meaning & Importance; Project Life Cycle, Project Scheduling, Capital Budgeting, Generating an Investment Project Proposal, Project Report-Need and Significance of Report, Contents, Formulation, Project Analysis-Market, Technical, Financial, Economic, Ecological, Project Evaluation and Selection, Project Financing, Project Implementation Phase, Human & Administrative aspects of Project Management, Prerequisites for Successful Project Implementation. New Control Techniques- PERT and CPM, Steps involved in developing the network, Uses and Limitations of PERT and CPM

Text Books:

1. P.C Tripathi, P.N Reddy, "Principles of Management", 6th Edition, McGraw Hill Education, 2017.
2. Poornima M Charantimath, "Entrepreneurship Development Small Business Enterprises", 2nd Edition, Pearson Education 2008.

References:

1. Vasant Desai, "Dynamics of Entrepreneurial Development and Management", 6th Revised Edition, Himalaya Publication House, 2018
2. Harold Koontz, Heinz Weihrich, "Essentials of Management: An International, Innovation and Leadership Perspective", 10thEdition, McGraw Hill Education, 2016.

Course Outcomes (COs):

1. Identify the importance of managerial discipline (POs – 1, 2, 3,4, 5, 6, 7, 8, 9, 10, 11, 12, PSO – 2, 3)
2. Interpret the concepts of directing and controlling for an organization (POs – 1, 2, 3,5, 7, 8, 9, 10, 11, 12, PSO – 2, 3)
3. Demonstrate the functions and acquire necessary skills to be a successful entrepreneur (POs – 1, 4, 5, 6, 7, 8, 9, 10, 11, 12, PSO – 2, 3)
4. Describe various polices and institutional supports in growth of Indian economy (POs – 1, 4, 5, 6, 7, 8, 9, 10, 11, 12, PSO –2, 3)
5. Recognize and prepare effectively project appraisal and report (POs – 3, 5, 6, 8, 9, 10, 11, 12, PSO – 3)

COMMUNICATION SYSTEMS LABORATORY– I

Course Code: ECL56 **Credits: 0:0:1**
Prerequisites: Analog Circuits Laboratory **Contact Hours: 28**
Course Coordinator: T. D. Senthilkumar

List of Experiments

1. Class-C tuned amplifier
2. Generation of standard AM
3. AM demodulation using envelope detector
4. Generation of DSBSC using ring modulation
5. Generation of direct FM
6. FM demodulation using PLL
7. Up conversion and down conversion using transistor mixer
8. Pre-emphasis and de-emphasis
9. Frequency division multiplexing (FDM)
10. Simulation of second order active low pass and high pass filter
11. Simulation of band pass and band reject filter
12. Simulation of analog modulation techniques

Text Books:

1. David A. Bell, "Operational Amplifiers and Linear ICs", 3rd Edition, PHI/Pearson, 2011.
2. J. G. Proakis and M. Salehi, "Contemporary Communication Systems using MATLAB", 1st Edition, PWS Publishing Company, 2007.
3. Cory L Clark, "Labview Digital Signal Processing and Digital Communications", 1st Edition, McGraw-Hill Education, 2014.

Course Outcomes (COs):

1. Simulate and implement modulation and demodulation circuits for AM and FM (POs – 1, 2, 3, 4, 5 ,8, 9, 10,12, PSOs – 1, 3)
2. Implement up and down converters using transistor mixer (POs – 1, 2, 3, 4, 5, 8, 9, 10,12 PSOs – 1, 3)
3. Implement pre-emphasis and de-emphasis circuits (POs – 1, 2, 3, 4, 5,8, 9, 10, 12, PSOs – 1, 3)
4. Implement RF class-c tuned amplifier of super heterodyne receiver (POs – 1, 2, 3, 4, 5, 8, 9, 10, 12, PSOs – 1, 3)
5. Simulate different types of filters used in radio transmitter and receiver (POs – 1, 2, 3, 4, 5, 8, 9, 10, 12, PSO – 3)

CMOS VLSI LABORATORY

Course Code: ECL57 **Credits: 0:0:1**
Prerequisites: -- **Contact Hours: 28**
Course Coordinator: Raghuram S

List of Experiments

1. Front End ASIC Design Flow – Combinational Circuits
2. Front End ASIC Design Flow – Sequential Circuits
3. V-I Characteristics of MOS Transistors
4. Characterization of MOS Transistors – VT0, Kp, Lambda, Mu calculation
5. CMOS Inverter Transient and DC Analysis
6. Basic gates – calculation of propagation delay
7. Inverter – layout: DRC, LVS
8. Inverter – layout: post-layout simulation
9. Carry Lookahead Adder – RTL Design and Synthesis
10. Calculation of FO4 delay
11. Inverter chain design
12. Dynamic Gates – design and delay calculation

Text Books:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuit and Systems Perspective", 4th Edition, Pearson Education, 2015.

References:

1. Jan Rabaey, B.Nikolic, A. Chandrakasan, "Digital Integrated Circuits: A Design Perspective", 2nd Edition, Pearson Education, 2003.
2. Morris Mano, Michael Ciletti, "Digital Design", 5th Edition, Pearson Education, 2013.

Course Outcomes (COs):

1. Employ the digital design tools for HDL design entry, simulation, and synthesis (POs – 2, 3, 4, 5, 8, 9, 10,12, PSO – 2)
2. Create and verify functionality of various gates at the transistor level (POs – – 2, 3, 4, 5,8, 9, 10,12, PSO – 2)
3. Measure circuit performance parameters by performing simulations of circuit configurations (POs – – 2, 3, 4, 5,8, 9, 10,12, PSO – 2)
4. Use tools to characterize processes by conducting suitable experiments (POs – – 2, 3, 4, 5,8, 9, 10,12, PSO – 2)
5. Create the layout for simple gates, and perform RC extraction and post layout simulation (POs – 2, 3, 4, 5,8, 9, 10,12, PSO – 2)

MICROWAVE AND ANTENNAS LABORATORY

Course Code: ECL58 **Credits: 0:0:1**
Prerequisites: Microwaves and Antennas **Contact hours: 28**
Course Coordinator: Sujatha B

List of Experiments

1. Determination of the modes, transit time, electronic timing range and sensitivity of Klystron source
2. Measurement of VSWR, guide wavelength, operating frequency and impedance of unknown load (Horn antenna)
3. Determination of V-I characteristics of GUNN diode, and measurement of guide wavelength, frequency and VSWR applying Gunn source
4. Determination of coupling coefficient and insertion loss of branch line and backward directional couplers (Microstrip components)
5. Determination of coupling coefficient and power division o f a hybrid tee (Magic tee)
6. Measurement of power division and isolation characteristics of a 3dB power divider
7. Measurement of resonant frequency and permittivity of a microstrip ring resonator
8. Measurement of coupling coefficient, isolation and insertion loss of a rectangular waveguide type directional coupler
9. Experimental studies on radiation pattern of Horn antenna and determination of its beam area, directivity and gain
10. Experimental studies of radiation pattern of microstripYagi-Uda antenna and determination of its beam area, directivity and gain
11. Experimental studies of radiation pattern of microstripdipole antenna and determination of its beam area, directivity and gain.
12. Design and simulation of a dipole antenna using HFSS

References:

1. David M. Pozar, "Microwave Engineering", 4th Edition, Wiley Publications, 2011.
2. Samuel Y Liao, "Microwave Devices and Circuits", 3rd Edition, Pearson Education, 2011.
3. John D Kraus, Ronald J Marhetka, Ahmad S Khan, "Antennas and Wave Propagation", 5th Edition, Tata McGraw Hill, 2017.

Course Outcomes (COs):

1. Analyze the characteristics of Multiport Microwave networks (POs –1, 2,4, 5, 6, 7, 8, 9, 10, 12, PSO – 3)
2. Interpret the characteristics of Microwave Oscillators and measure the impedance of unknown load (POs – 1, 2,4, 5, 6, 7, 8, 9, 10,12, PSO – 3)
3. Construct the radiation pattern and calculate the antenna parameters (POs – 1, 2,4, 5, 6, 7, 8, 9, 10,12, PSO – 3)
4. Measure the resonant frequency of ring resonator and analyze its permittivity (POs –1, 2,4, 5, 6, 7, 8, 9, 10,12, PSO – 3)
5. Analyze V-I characteristics of GUNN diode (POs –1, 2,4, 5, 6, 7, 8, 9, 10,12, PSO – 3)

ANALOG AND MIXED SIGNAL VLSI DESIGN

Course Code: EC61 **Credits: 3:1:0**
Prerequisites: Analog Circuits **Contact Hours: 70**
Course Coordinator: M. Nagabushanam

UNIT – I

Introduction and Single Stage Amplifiers: MOS device basics, MOS device models, RC circuits, Passive devices, mixed signal layout issues, Common Source Amplifiers, Source Follower, Common Gate, Cascode Structures and Folded Cascade Structures

UNIT – II

Differential Amplifier and Current Mirrors: Introduction to Differential Pair Amplifier, Quantitative Analysis to Differential Pair Amplifier, Common Mode Response, Differential Amplifiers with Different Loads, Effects of mismatches. Simple Current Mirrors, Cascode Current Mirrors, Differential Pair with Current Mirror Load

UNIT – III

Operational Amplifiers and Frequency Response: Op Amps Low Frequency Analysis, Telescopic Op Amps, Folded Cascode Op Amps, Two Stage Op Amps, Common Mode Feedback, Frequency Response of Common Source Amplifiers, Differential Amplifiers, Single Ended Differential Pair

UNIT – IV

Data Converter Fundamentals: Analog versus Discrete Time Signals, Converting Analog Signals to Digital Signals, Sample-and-Hold Characteristics, Digital-to-Analog Converter Specifications, Analog-to-Digital Converter Specifications, Mixed-Signal Layout Issues

UNIT – V

DAC and ADC Architectures: Digital Input Code, Resistor String, R-2R Ladder Networks, Current Steering, Charge Scaling DACs, Cyclic DAC, Pipeline DAC, ADC Architectures: Flash ADC, Two-Step Flash ADC, Pipeline ADC, Integrating ADCs, Successive Approximation ADC, Oversampling ADC

Text Books:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Education (India) Edition, 2018.
2. R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation", 3rd Edition, John Wiley & Sons. Inc., Publishing, 2010.

References:

1. P E Allen and D R Holberg, "CMOS Analog Circuit Design", 2nd Edition, Oxford University Press, 2002.
2. Behzad Razavi, "Fundamentals of Microelectronics", 1st Edition, Wiley Publishing, 2008.

Course Outcomes (COs):

1. Employ the concept of MOS devices in various MOS amplifier configurations (POs – 1, 2, 3, 4, 8, 12, PSO – 2)
2. Design differential amplifiers with different MOS loads. (POs – 1, 2, 3, 4, 8,12, PSO – 2)
3. Construct one/two stage opamp and analyze the frequency response of opamps. (POs – 2, 3, 4, 8,12, PSO – 2)
4. Define various specifications of ADCs/DACs (POs – 2, 3, 4, 8, PSO – 2)
5. Illustrate different types of ADC and DAC architectures (POs – 2, 3, 4,8, PSO – 2)

EMBEDDED SYSTEM DESIGN

Course Code: EC62 **Credits: 3:1:0**
Prerequisites: Microprocessors **Contact Hours: 70**
Course Coordinators: Lakshmi Shrinivasan, Suma K V

UNIT – I

Typical Embedded Systems: Core of the embedded system, memory, sensors and actuators, communication interface, other system components, characteristics and quality attributes of embedded systems

UNIT – II

Hardware Side – An Introduction: Instructions, registers, embedded systems – an instruction set view, register view, register transfer language, and register view of a microprocessor, fundamental issues in hardware software co-design, computational models in embedded systems, The interrupt, interrupt service routine, interrupt vector table, control of the interrupt table.

UNIT – III

Programming for Embedded Systems: Overview of ANSI C, GNU development tools, bit manipulation using C, memory management, timing of programs, device drivers, productivity tools, code optimization, C coding guidelines, Types of file generated on cross compilation, disassembler/decompiler, simulators, emulators and debugging, target hardware debugging, boundary scan

UNIT – IV

GPIO and Interfacing: General purpose input/output ports, Interfacing of ADC, DAC, UART, I2C, LCD, stepper motor, LED, keypad and 7-segment display using data sheets of a microcontroller

UNIT – V

RTOS and IDE for Embedded System Design: Operating system basics, types of operating systems, task, process and threads, thread preemption, preemptive task scheduling techniques, task communication, task synchronization issues – racing and deadlock, concept of binary and counting semaphores, how to choose an RTOS, System programming**:** processes, signals, multithreading and semaphores

Text Books:

1. Dr. K. V. K. K. Prasad, “Embedded Real-Time Systems: Concepts, Design & Programming”, Reprint Edition, Dreamtech Press, 2013.
2. Shibu K. V, “Introduction to Embedded Systems”, 2nd Edition, Tata McGraw Hill Education, 2017.
3. James K. Peckol, “Embedded Systems – A Contemporary Design Tool”, Student Edition, John Wileyand Sons, 2014.

References:

1. Steve Heath, "Embedded System Design", 2nd Edition, Newnes Publishers, 2003.
2. LPC 2148 user manual.

Course Outcomes (COs):

1. Identify the requirements of an embedded system (POs – 1, 3, 8, PSO – 2)
2. Understand the hardware architecture in an embedded systems (POs – 1, 2, 3,4, 8, 12, PSO – 2)
3. Develop and debug embedded C programs (POs –1, 2, 3, 4, 5, 8, 12, PSO – 2)
4. Design an embedded system using different peripherals (POs –2, 3, 4, 5, 8, 12, PSO – 2)
5. Illustrate RTOS concepts in embedded system design (POs –1, 2,4, 5, 8, 12, PSO – 2)

MINI PROJECT/PROFESSIONAL ELECTIVE/NPTEL COURSE

Course Code: EC65 **Credits: 0:0:4**

Contact Hours: 5

EVALUATION RUBRICS FOR MINIPROJECT

Criteria	Max. Marks	Achievement Levels			Marks Awarded	CO Mapping
		Inadequate (0% - 33%)	Development (34% - 66%)	Proficient (67% - 100%)		
Introduction to Area (Review I)	**10**	No information about the specific technical details in the area	Some information about the area, but no clarity in internal details	Clear presentation of the technical working, and chosen area and rationale of design choices		**CO1**
Explanation of Technical Block Diagram	**10**	Block diagram is technically incorrect or is not practical	Technically correct block diagram but not feasible in practical settings	Technical correct block diagram with tools and resources for implementation available		**CO2**
Implementation of Block Diagram	**10**	Incomplete implementation of block diagram	Block diagram is implemented but results not generated	Block diagram is complete, with results matching reference works		**CO3**
Results & Discussion	**10**	No results and no functionality generated	Results generated, but not in a comprehensive manner	Results generated along with Design of Experiments for comprehensive testing		**CO4**
Report Writing	**10**	Proper technical language not used	Proper technical language along with flow from beginning to end	Technical language, flow, and graphical elements used extensively to express hypotheses		**CO5**

EVALUATION RUBRICS FOR MOOC

Evaluation Component	Achievement Levels			CO Mapping
	Satisfactory	Good	Excellent	
Assignment (Max. Marks = 30)	Not all assignments attempted, average score less than 50% (0 – 10)	All assignments attempted with at least an average score of 50% (10 – 20)	All assignments completed with average score > 70% (20 – 30)	**CO1, CO2, CO3**
Exam (Max. Marks = 20)	Attempted Exam but not cleared (0 – 10)	Attempted Exam and passed with at least a score of 50% (10 – 20)	Attempted Exam and passed with score > 70% (20)	**CO4, CO5**

Course Outcomes (COs):

1. Demonstrate a basic knowledge in the chosen domain (POs – 1, 2, 3, 4, 6,7, 8, 9, 10, 11, 12, PSO – 1)
2. Describe concepts in an accurate manner (POs – 2, 3, 8, 9, 10, 11, PSOs – 2, 3)
3. Discuss technical issues in the chosen domain (POs – 2, 3, 4, 5, 6,7 ,8, 9, 10, 11, PSOs – 2, 3)
4. Propose technical solutions to practical problems/bottleneck in the chosen domain (POs –1 2, 3, 4, 5, 6, 7, 9, 10, 12, PSOs – 2, 3)
5. Create a technical document expressing the details of work done (POs – 8, 9, 10,12, PSOs – 2, 3)

COMMUNICATION SYSTEMS LABORATORY – II

Course Code: ECL66 **Credits: 0:0:1**
Prerequisites: Communication Systems Laboratory – I **Contact Hours: 28**
Course Coordinator: T. D. Senthilkumar

List of Experiments

1. Verification of sampling theorem
2. Time division multiplexing
3. Generation and detection of amplitude shift keying signals
4. Generation and detection of frequency shift keying signals
5. Generation and detection of phase shift keying signals
6. Generation and detection of quadrature PSK and DPSK
7. PCM modulation and demodulation
8. Delta modulation and demodulation
9. Simulation for verification of sampling theorem
10. Simulation of line coding techniques
11. Performance analysis of ASK, FSK and PSK

Text Books:

1. Simon Haykin, "Digital Communications", John Wiley, Reprint 2014.
2. J. G. Proakis, M. Salehi, "Contemporary Communication Systems using MATLAB", 1st Edition, PWS Publishing Company, 2007.
3. Cory L Clark, "Labview Digital Signal Processing and Digital Communications", 1st Edition, McGraw Hill Education, 2016.

Course Outcomes (COs):

1. Implement a sampling circuit to verify Nyquist theorem (POs – 1, 2, 3, 4, 5, 6, 8, 9, 10, 12, PSO – 3)
2. Employ TDM for band limited signals (POs – 1, 2, 3, 4, 5, 8, 9, 10, 12, PSO – 3)
3. Implement ASK, PSK, FSK, DPSK digital modulation schemes (POs – 1, 2, 3, 4, 5, 8, 9, 10, 12, PSO – 3)
4. Implement PCM and delta modulation scheme (POs – 1, 2, 3, 4, 5, 7, 8, 9,10, 12, PSO – 3)
5. Analyze the performance of various digital modulation techniques (POs – 1, 2, 3, 4, 5, 8, 9, 10, 12 PSO – 3)

ANALOG AND MIXED SIGNAL VLSI LABORATORY

Course Code: ECL67 **Credits: 0:0:1**
Prerequisites: CMOS VLSI **Contact Hours: 28**
Course Coordinator: M. Nagabushanam

List of Experiments

Design the following analog circuits with the given specifications and complete the design flow. Draw the schematic and perform DC Analysis, AC Analysis, Transient Analysis and frequency response.

1. CMOS inverter
2. Current mirror
3. Common source amplifier with current mirror
4. Common drain amplifier with current mirror
5. Common gate amplifier
6. Differential amplifier
7. Single stage op-amp
8. Two stage op-amp
9. 4-bit R-2R DAC
10. 2-bit Flash ADC

Textbooks:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGrawHill Education, 2018.
2. R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation", 3rd Edition John Wiley & Sons Inc., Publishing, 2010.
3. P. E. Allen, D R Holberg, "CMOS Analog Circuit Design", 2nd Edition, Oxford University Press, 2002.

Course Outcomes (COs):

1. Construct CMOS inverter and perform DC and transient analysis (POs –1, 2, 3, 4, 5, 8, 9, 10, 12, PSO – 2)
2. Develop a current mirror circuit and analyze its performance. (POs –1, 2, 3, 4, 5, 8, 9, 10, 12 PSO – 2)
3. Utilize the current mirror circuit as load for single stage amplifier configuration and perform AC and transient analysis (POs –1, 2, 3, 4,5, 8, 9, 10, 12, PSO – 2)
4. Develop a single stage/two stage opamp circuit and study its performance. (POs –1, 2, 3, 4, 5,8, 9, 10, 12, PSO – 2)
5. Design an N-bit ADC/DAC and evaluate its characteristics. (POs – 1, 2, 3, 4, 5, 8, 9, 10, 12, PSO – 2)

EMBEDDED SYSTEM DESIGN LABORATORY

Course Code: ECL68 **Credits: 0:0:1**
Prerequisites: Microprocessor Laboratory **Contact Hours: 28**
Course Coordinator: Lakshmi Shrinivasan, Suma K V

List of Experiments

Part A: Embedded C programming

1. Bit manipulation
2. Calculation of Cyclic Redundancy Code
3. Device driver for reading from keyboard and writing to monitor using system calls

Part B: RTOS Programs (System level programming by Linux API)

1. Creation of processes using fork()
2. Usage of 'Signal' function calls – when DEL key or CTRL C is pressed, this sends a signal for abrupt termination
3. Multithreading – One thread reads the input from the keyboard and another thread converts to upper case. This is done until 'Stop' is pressed.Number of threads can be running sharing same CPU.
4. Intertask communication using semaphore and pipes – Two threads, one for reading the input and one for converting the text to upper case letters, converting thread will wait for a semaphore to be released before it starts the operation and also pipes can be used to share the data from one thread to another

Part C: Interfacing programs

1. Familiarize I/O ports of a controller – on/off control of LEDs using switches.
2. Display a given string using the LCD display interface.
3. Interface keypad and display the key pressed on LCD.
4. Waveform generation using the internal DAC of LPC 2148
5. Convert a given analog voltage to digital using ADC of LPC 2148
6. Interface a stepper motor and control the speed of it
7. Design and display a two-digit counter (using timer/counter/capture module of LPC 2148)

Textbooks:

1. Dr. K. V. K. K. Prasad, "Embedded Real-Time Systems: Concepts, Design & Programming", Reprint Edition, Dreamtech Press, 2013.
2. LPC 2148 user manual.

Course Outcome (COs):

1. Develop embedded C programs (POs – 1, 2, 3, 4, 5, 8, 9, 10, 12, PSO – 2)
2. Demonstrate embedded C programs to create process/tasks and threads for RTOS (POs – 1, 2, 3, 5, 8, 9, 10, 12, PSO – 2)
3. Illustrate inter-task communication using embedded C programs (POs – 1, 2, 3, 5, 8, 9, 10, 12, PSO – 2)
4. Design embedded C programs to interface data converters with a microcontroller (POs – 1, 2, 3, 5, 6, 8, 9, 10, 12, PSO – 2)
5. Interface different types of I/O peripherals using a microcontroller for a typical application (POs – 1, 2, 3, 4, 5, 8, 9, 10, 12, PSO – 2)

DEPARTMENT ELECTIVES

V SEMESTER (ELECTIVE I)

INFORMATION, LEARNING AND INFERENCE

Course Code: ECE551 **Credits: 3:0:0**
Prerequisites: Engineering Mathematics **Contact Hours: 42**
Course Coordinator: Sara Mohan George

UNIT – I

Probability, Entropy and Inference: Probabilities and ensembles, Meaning of probability, Forward and inverse probabilities, Gibb's inequality, Jensen's inequality for convex functions, Inference, Random variables

UNIT – II

Linear Algebra: Systems of linear equations, Matrices, Solving systems of linear equations, Vector spaces, Linear Independence, Basis and Rank, Change of basis

UNIT – III

Matrix Decomposition: Determinant and Trace, Eigen Values and Eigen Vectors, Cholesky decomposition, Eigen decomposition and diagonalization, Singular Value Decomposition (SVD)

UNIT – IV

Analytic Geometry: Norms, Inner product, Lengths and Distances, Angles and Orthogonality, Orthogonal Basis, Orthogonal Projections, Rotations

UNIT – V

Continuous Optimization: Optimization using Gradient Descent, Constrained optimization and Lagrange multipliers, Convex optimization.

Text Books:

1. David J. C. MacKay, "Information Theory, Inference and Learning Algorithms", Cambridge University Press, 2003.
2. M. P. Deisenroth, A. A. Faisal, C. S. Ong, "Mathematics for Machine Learning", 1st edition, Cambridge University Press, 2020.

References:

1. A. Papoulis, S. Unnikrishna Pillai, "Probability, Random Variables and Stochastic Processes", 4th Edition, McGraw Hill, 2002.
2. David C Lay, Stephen R Lay, Judi J McDonald, "Linear Algebra and its Applications", 5thEdition, Pearson Education, 2015.
3. Stephen Boyd, Lieven Vandenberghe, "Convex Optimization", Cambridge University Press, 2004.

Course Outcomes (COs):

1. Appraise basics of probability and entropy (POs – 1, 2, 3, 8, 12, PSO – 3)
2. Solve systems of linear equations using multiple methods and demonstrate understanding of the concepts of vector space (POs – 1, 2, 3, 8,12 PSO – 3)
3. Apply principles of matrix algebra and orthogonality to transformations (POs –1, 2, 3, 8, 12, PSO– 3)
4. Compute and interpret eigenvalues and eigenvectors, orthogonality and diagonalization (POs – 1, 2, 3, 5, 8, 12, PSO – 3)
5. Formulate optimization problems for given situations and apply different methods of optimization. (POs – 1, 2, 3, 5, 8, 12, PSO – 3)

ADVANCED DIGITAL DESIGN

Course Code: ECE552 **Credits: 3:0:0**
Prerequisites: Digital Design **Contact Hours: 42**
Course Coordinator: Reshma Verma

UNIT – I

Current trends in VLSI design: Technology scaling, Die size growth, Frequency, Power dissipation, Challenges in digital design, Design metrics, Cost of integrated circuits, ASIC, Evolution of SoC, ASIC flow vs SoC flow, SoC design challenges

Introduction to Verilog: Lexical Conventions, Data Types, Modules, Nets, Values, Data Types, Comments and arrays in Verilog, Expressions, Operators, Operands, Arrays, memories, Strings, Gate level modeling examples, Data flow modeling examples, Operator types.

UNIT – II

RTL Design using Verilog: Behavioral coding, Procedural blocks, Blocking and Non-Blocking assignment, looping, flow control, Basic test bench generation and simulation, Verilog coding guide lines for combinational, sequential designs, General guidelines, Sensitivity list, RTL design challenges, Verilog modeling of combinational logic, Verilog modeling of sequential logic

UNIT – III

Verilog Tasks and Functions: Difference between Task and Function, coding examples using Task, Coding example using Function.

Synchronous Sequential Circuits: Basic steps, State assignment problems, Mealy state model, Verilog description for Mealy and Moore type FSM, FSM for serial adder (Mealy, Moore type), Verilog description, State minimization, Incompletely specified FSMs, Design of a counter using sequential circuit approach

UNIT – IV

Logic Synthesis with Verilog HDL: Meaning of logic synthesis, Impact of logic synthesis, Verilog HDL synthesis, Synthesis design flow, Modeling tips for logic synthesis

Synthesis of Verilog Constructs to Gates: Synthesis of different operators, Conditional expression, always statement, If statement, Case statement, loop statement, Modeling flipflops, Gate level modeling, Module instantiations**,** examples of combinational logic description, Sequential logic description. Synthesis of FSMs

UNIT – V

Case Study: Accelerators: General Concepts, Video Edge Detection, Verifying an Accelerator

Design Methodology: Architecture exploration, Functional design, Functional verification, Synthesis, Physical area optimization, Timing optimization, Power optimization

Text Books:

1. Samir Palnitkar, "Verilog HDL – A Guide to Digital Design and Synthesis", 2nd Edition, Pearson Education, 2017.
2. Stephen Brown, Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design",3rd Edition, Tata McGrawHill, 2014.
3. J. Bhasker, "Verilog HDL Synthesis: A Practical Primer", 3rd Edition, Star Galaxy, 2018.
4. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach using Verilog", Elsevier, 2010.

References:

1. Morris Mano, Michael Ciletti, "Digital Design", 5th Edition, Pearson Education, 2013.
2. Seer Academy Recordings

Course Outcomes (COs):

1. Appraise the present scenario in VLSI design and the need for the use of Verilog to develop hardware description (POs – 1, 2, 3, 6, 8, 12, PSO – 2)
2. Employ coding skills to model sequential and combinational circuits using behavioral style Verilog coding (POs –1, 2, 3, 4, 8, 12 PSO – 2)
3. Demonstrate the use of finite state machines to design digital circuits and use Verilog code to model them (POs –1, 2, 3, 4, 8, 12, PSO – 2)
4. Explain the impact of logic synthesis and interpret how each Verilog construct gets synthesized into its hardware equivalent (POs –1, 2, 3, 4, 8, 12, PSO – 2)
5. Understand the CAD flow and optimization tradeoffs in digital systems for ASIC/FPGA implementation (POs – 1, 2, 3, 4, 5, 8, 12, PSO – 2)

OPERATING SYSTEMS

Course Code: ECE553 **Credits: 3:0:0**
Prerequisite: Data Structures using C++ **Contact Sessions: 42**
Course Coordinators: Deepali B Koppad, Mamtha Mohan

UNIT– I

Introduction to Operating Systems: VM based operating systems, Kernel based operating systems, Microkernel based operating systems, Distributed systems

Scheduling: Introduction, First In, First Out (FIFO), Shortest Job First (SJF), Shortest Time-to-Completion First (STCF), Round Robin

UNIT – II

Process Synchronization: Avoidance and Concurrency: Introduction, Thread creation, Thread completion

Deadlocks: Deadlocks in resource allocation, Resource state modeling, Deadlock detection algorithm (Avoidance), Deadlock prevention

.

UNIT – III

Paging and Segmentation: Introduction, Page table, Smaller tables**,** Hybrid approach: Paging and Segments, Multi-level page tables segmentation, Generalized base/bounds

File Systems and Directories: File system interface, Making, Reading and deleting directories, File system implementation, Inode, Directory organization, Free space management

UNIT – IV

Forensics and Operating Systems: Introduction, Forensics, Memory forensics – real memory and addressing, Virtual memory

Mobile Operating Systems: Introduction, Encryption and Remote Control, Rooting/Jailbreaking, Android, BlackBerry, IOS and Windows Mobile

UNIT – V

Tracking Artifacts: Introduction, Location information, Document tracking, shortcuts

Newer Technologies: Introduction, Virtualization, Cloud Computing, Wearables, Drones

Text Books:

1. Remzi Arpaci-Dusseau, Andrea Arpaci-Dusseau, “Operating Systems: Three Easy Pieces”, 1st Edition, Arpaci-Dusseau Books, 2015.
2. Ric Messier, “Operating Systems Forensics”, 1st Edition, Elsevier Inc., 2015.

References:

1. William Stallings , “Operating Systems: Internals and Design Principles”, 8th Edition, Pearson Education, 2014.
2. A. Silberschatz, Peter B. Galvin, G. Gagne, “Operating System Concepts”, 9thEdition, Wiley, 2012.

Course Outcomes (COs):

1. Enumerate different types of OS and scheduling algorithms. (PO – 1, 2, 8, 12, PSO – 3)
2. Illustrate process synchronization and deadlock avoidance. (POs – 1, 2, 8, 12, PSO – 3)
3. Elaborate on segmentation and file system organization. (POs – 1, 2, 8, 12, PSO – 3)
4. Acquire knowledge of forensics in mobile operating systems. (POs – 1, 2, 8, 12, PSO – 3)
5. Obtain innovative knowledge of newer technologies. (POs – 1, 2, 8, 12, PSO – 3)

COMPUTER ARCHITECTURE

Course Code: ECE554 **Credits: 3:0:0**
Prerequisites: Digital Design **Contact Hours: 42**
Course Coordinators: V. Anandi, Raghuram S

UNIT – I

Introduction: Combinational and Sequential logic circuits, Computer systems, Technologies for building processors and memory, Uniprocessors and Multiprocessors

Instruction Sets: Computer hardware, Representing instructions in the computer, Instructions for making decisions, Sample instruction sets

UNIT – II

Computer Arithmetic: Addition and Subtraction, Multiplication, Division, Floating point parallelism and computer arithmetic

The Processor: Introduction, Logic design conventions, Building a data path, A simple implementation scheme, Overview of pipelining, Pipelined data path, Hazards, Exceptions

UNIT – III

Memory Hierarchy: Introduction, Memory technologies, Basics of caches, Measuring and improving cache performance, Memory hierarchy, Virtual machines, Virtual memory, ARM CortexA53 and Intel Core i7, Memory hierarchies

UNIT – IV

Parallel Processors from Client to Cloud: Introduction, Parallel processing programs, SISD, MIMD, SIMD, SPMD, Vector, Hardware multithreading, Multicore and other shared memory multiprocessors, Multiprocessor benchmarks and performance models

UNIT – V

Graphics and Computing GPUs: Introduction, GPU system architectures, Programming GPUs, Multithreaded multiprocessor architecture, Parallel memory system, Floating point arithmetic, NVIDIA GeForce 8800 B-46, Mapping applications to GPUs

Text Books:

1. David A Patterson, John L Hennessey, “Computer Organization and Design: The Hardware Software Interface, The Morgan Kaufmann [RISC-V Edition] 2017.

References:

1. Kai Hwang and Zu, “Scalable Parallel Computers Architecture” 1st Edition, Tata McGraw Hill, 2003.
2. M.J Flynn, “Computer Architecture: Pipelined and Parallel Processor Design”, Jones & Bartlett Learning, 1995.

3. D.A. Patterson, J.L. Hennessey, “Computer Architecture: A Quantitative Approach”, 5th Edition, Morgan Kaufmann, 2012.

Course Outcomes (COs):

1. Understand contemporary computer architecture issues and techniques. (POs – 1, 2, 6, 8, 12, PSO – 2)
2. Design basic and intermediate RISC pipelines, including the instruction set, data paths, and ways of dealing with pipeline hazards. (POs – 1, 2, 3, 4, 8, 12, PSO – 2)
3. Understand memory hierarchy design virtual memory, caches and virtual machines. (POs – 1, 2, 3, 5, 8, 12, PSO – 2)
4. Compare properties of shared memory and distributed multiprocessor systems and cache coherency protocols. (POs –1, 2, 3, 6, 8, 12, PSO – 2)
5. Explain multithreading architectures, the methods for designing speculative multithreading processors and GPU. (POs – 1, 2, 3, 6, 8, 12, PSO – 2)

VI SEMESTER (ELECTIVE II)

IMAGE AND VIDEO PROCESSING

Course Code: ECE631 **Credits: 3:0:0**
Prerequisites: Digital Signal Processing **Contact Hours: 42**
Course Coordinator: K. Indira

UNIT – I

Fundamentals and Intensity Transformations: Image sensing and acquisition, Image sampling and quantization, Some basic relationship between pixels, Basics of intensity transformations and spatial filtering, Basic intensity transformation functions, Histogram processing, Mechanics of spatial Filtering, Smoothing and Sharpening spatial filters.

UNIT – II

Filtering in Frequency Domain: Basics of filtering in frequency domain, Image smoothing using low pass frequency domain filters – Ideal, Gaussian, and Butterworth low pass filters, Image sharpening using high pass filters – Ideal, Gaussian, and Butterworth high pass filters

Image Transforms: Discrete Cosine and Wavelet Transforms

UNIT – III

Image Segmentation: Fundamentals, line detection, edge detection, basic global thresholding, multiple thresholds, variable thresholding, region growing, region splitting and merging

Object Recognition: Patterns and pattern classes, Recognition based on decision theoretic methods, matching and optimum statistical classifier

UNIT – IV

Basic of Digital Video: Digital video signal, Digital video standards, sampling structures for digital video

Two-Dimensional Motion Estimation: The correspondence problem and optical flow estimation, Motion Estimation is ill-posed: aperture and occlusion problems, Block based methods: Hierarchical Motion Estimation

UNIT – V

Video Segmentation and Tracking: Motion segmentation using direct method: Thresholding for change detection and algorithm using mapping parameters

Motion Tracking: Basic principles, 2D motion tracking

Text Books:

1. R C. Gonzalez, R.E. Woods, “Digital Image Processing”, 4th Edition, Pearson Education 2018.
2. A. Murat Tekalp, “Digital Video Processing”, 1st Edition, Pearson Education Inc., 1995.

References:

1. Anil. K. Jain, “Fundamentals of Digital Image Processing”, Prentice Education, 2002.
2. R. C. Gonzalez, R. E. Woods, S. L. Eddins, “Digital Image Processing using MATLAB”, 2nd Edition, Pearson Education, 2017.

Course Outcomes (COs):

1. Analyze general terminology of digital image processing and employ basic intensity transformation functions. (POs – 1, 2, 3, 5, 8, 12, PSO – 3)
2. Interpret smoothing and sharpening of images using frequency domain filters and appreciate various image transforms. (POs –1, 2, 3, 5, 8,12, PSO – 3)
3. Evaluate the methodologies for segmentation and classification of objects in an image. (POs – 1, 2, 3, 5, 8, 12, PSO – 3)
4. Appraise different models for video processing and motion estimation. (POs – 1, 2, 3, 5, 8, 12 PSO – 3)
5. Apply video processing techniques in practical applications. (POs – 1, 2, 3, 4, 5, 8,12, PSO – 3)

ADVANCED DIGITAL LOGIC VERIFICATION

Course Code: ECE632 **Credits: 3:0:0**
Prerequisites: Digital Design **Contact Hours: 42**
Course Coordinator: Deepali B Koppad

UNIT – I

Verification Concepts: Concepts of Verification, Importance of verification, Stimulus vs Verification, Test bench generation, Functional verification approaches, Typical verification flow, Stimulus generation, Direct testing, Coverage: Code coverage and Functional coverage, Coverage plan

UNIT – II

System Verilog – Language Constructs: System Verilog Constructs – Data types: Two state data, Strings, Arrays: Queues, Dynamic and Associative arrays, Structs, Enumerated types. Program blocks, modules, interfaces, Clocking ports, Mod ports

UNIT – III

System Verilog – Classes and Randomization: SV classes: Language evolution, Classes and Objects, Class Variables and Methods, Class Instantiation, Inheritance and Encapsulation, Polymorphism, Randomization: Directed vs Random testing, Randomization, Constraint driven randomization

UNIT – IV

System Verilog – Assertions and Coverage: Assertions: Introduction to assertion based verification, Immediate and concurrent assertions, Coverage driven assertion, Motivation, Types of coverage, Cover group, Cover point, Cross coverage, Concepts of binning and event sampling

UNIT – V

Test bench: Layered test bench architecture, Introduction to Universal Verification Methodology (UVM), Overview of UVM, Base classes and simulation phases in UVM, UVM environment structure, Connecting DUT – Virtual Interface

Text Books:

1. Chris Spear, Greogory J Tumbush, "System Verilog for Verification – A Guide to Learning Test Bench Language Features", Springer, 2012.
2. Stuart Sutherland, "RTL Modeling with System Verilog for Simulation and Synthesis: using System Verilog for ASIC and FPGA Design", 1st Edition, Create Space Independent Publishing Platform, 2017.

References:

1. System Verilog 3.1a LRM, Accellera's Extensions to Verilog
2. Sasan Iman, "Step by Step Functional Verification with System Verilog and OVM", Hansen Brown Publishing, 2008.
3. UVM Cookbook, Mentor Graphics
4. www.asic-world.com

5. www.testbench.in
6. www.chipverify.com/systemverilog/systemverilog-class
7. www.chipverify.com/uvm/uvm-tutorial
8. Seer Academy Recordings

Course Outcomes (COs):

1. Express the principles of HDL verification. (POs – 1, 2, 3, 4, 5, 8, 12, PSO – 2)
2. Apply OOPs concepts in System Verilog verification environment. (POs – 1, 2, 3, 4, 5, 8, 12, PSO – 2)
3. Construct basic verification environment using System Verilog (POs – 1, 2, 3, 4, 5, 8, 12, PSO – 2)
4. Generate random stimulus and track functional coverage using System Verilog (POs – 1, 2, 3, 4, 5, 8, 12, PSO – 2)
5. Appreciate the concepts of layered test bench architecture and its components (POs – 1, 2, 3, 4, 5, 8, 12, PSO – 2)

ERROR CONTROL CODING

Course Code: ECE633 **Credits: 3:0:0**
Prerequisites: Engineering Mathematics **Contact Hours: 42**
Course Coordinator: V. Nuthan Prasad

UNIT – I

Information Channels: Communication channels, Channel models, Channel matrix, Joint probability matrix, Mutual information, Channel capacity, Special channels, Capacity of: Binary symmetric channel, Binary erasure channel, Muroga's theorem

UNIT – II

Error Control Coding: Introduction, Linear block codes: Matrix description of linear block codes, Error detection and correction capabilities of linear block codes, Single error correcting Hamming codes, Table lookup decoding using standard array

UNIT – III

Binary Cyclic Codes: Algebraic structure of cyclic codes, Encoding using an (n – k) bit shift register, Syndrome calculation, Error detection and correction

UNIT – IV

Convolution Codes: Convolution encoder, Time domain approach, Transform domain approach, Code tree, Trellis and State diagram

UNIT – V

Turbo Codes: Introduction, Distance properties, Design of Turbo codes, Iterative decoding of Turbo codes: LogMAP algorithm and max LogMAP algorithm

Text Books:

1. K. Sam Shanmugham, "Digital and Analog Communication Systems", John Wiley Publications, 1996
2. Ranjan Bose, "Information Theory Coding and Cryptography", 2nd Edition, TMH Publication, 2007.
3. Shu Lin, Daniel J. Costello, "Error Control Coding", 2nd Edition, Prentice Hall, 2004.

References:

1. Bernard Sklar, "Digital Communications", Pearson Education, 2007.
2. Muralidhar Kulkarni, "Information Theory and Coding", 1st Edition, Wiley Publications, 2015.

Course Outcomes (COs):

1. Categorize various channels for information transmission and interpret Shannon's theorem. (POs – 1, 2, 3, 4, 8, 12, PSOs – 2,3)
2. Design linear block codes for error detection and correction (POs –1, 2, 3, 4, 8, 12, PSOs – 2, 3)
3. Model cyclic block codes using shift register for error detection and correction. (POs – 1, 2, 3, 4, 8, 12, PSO – 2, 3)
4. Construct trellis diagrams for convolution encoders (POs –1, 2, 3, 4, 5, 8, 12, PSOs – 2,3)
5. Apply various algorithms for decoding turbo codes (POs – 1, 2, 3, 4, 5, 8, 12, PSOs – 2,3)

ROBOTICS

Course Code: ECE634 **Credits: 3:0:0**
Prerequisites: Control Systems **Contact Hours: 42**
Course Coordinators: Flory Francis, Punya Prabha V

UNIT– I

Basic Concepts: Definition of robotics, Robotic architecture, Classification of robots, Industrial applications

Actuators and Grippers: Electric actuator, Hydraulic, Pneumatic, Electric drives

UNIT – II

Internal and External Sensors: Internal sensors, Position sensors, Incremental encoder, Absolute encoder, Resolver velocity sensors, Tachometer and hall effect sensor, Acceleration and forces sensors, Hall effect, Touch sensors, Proximity sensors, Ultrasonic sensors, Laser sensors for range measurements, Machine vision sensors

UNIT – III

Transformation: Rotation matrix, Composite rotation matrix, Rotation matrix with Euler angles representation, Homogenous transformation matrix, DH representation, Homogenous transformation for various arm configurations

UNIT – IV

Robotic Operating System (ROS): Introduction to OpenCV, OpenNI, PCL – Programming Kinect with Python using ROS, OpenCV, OpenNI– Point clouds using Kinect, ROS, OpenNI, PCL

UNIT – V

Interfacing with ROS: Building ChefBot hardware, ROS Python driver for ChefBot, ChefBot ROS launch files, Chef Bot Python nodes and launch files, Calibration and testing of Chef Bot

Text Books:

1. S K Saha, “Introduction to Robotics”, 2nd Edition, McGraw Hill Education Pvt. Ltd, 2008.
2. S Fu, R C Gonzalez, C S G Lee, “Robotics Control, Sensing Vision and Intelligence”, 3rd Edition, McGraw Hill International, 2016.
3. Lentin Joseph, “Learning Robotics using Python”, 2ndEdition, PACKT Publishing, 2015.

References:

1. Mikell P, Weiss G M, Nagel R N, “Industrial Robotics: Technology, Programming, and Applications”, 2nd Edition, McGraw Hill International, 2012.
2. A. Martinez, E. Fernandez, “Learning ROS for Robotics Programming”, PACKT Publishing, 2013.

Course Outcomes (COs):

1. Appreciate the architecture and applications of robots (POs – 1, 2, 3, 4, 8, 12, PSO – 1)
2. Analyze the principles of various sensors and their applications in robots (POs – 1, 2, 3, 4, 6, 8, 12 PSO – 1)
3. Apply DH parameter and homogenous transforms for robotic applications (POs –1, 2, 3, 4, 8, 12 PSO – 1)
4. Acquire knowledge ROS. (PO – 1, 2, 3, 5, 8, 12, PSO – 1)
5. Describe hardware design of Chef Bot. (PO – 1, 2, 3, 5, 8, 12, PSO – 1)

VI SEMESTER (ELECTIVE III)

RADARS AND SATELLITE COMMUNICATION

Course Code: ECE641 **Credits: 3:0:0**
Prerequisites: Microwaves and Antennas **Contact Hours: 42**
Course Coordinator: Sujatha. B

UNIT – I

Introduction to Radar: Basic radar – Principle of operation, Simple form of the radar equation, Maximum unambiguous range of radar, Radar block diagram, Radar frequencies, Applications of radar, Origin of radar

Radar Equation: Introduction, Range performance, Detection of signals in noise, Receiver noise and signal-to-noise ratio, Radar cross-section of targets, Pulse repetition frequency

UNIT – II

Doppler Radar: Doppler effect, CW Doppler radar, Delay line cancellers, Filter characteristics of delay-line canceller, Blind speeds, Clutter attenuation, Blind phases, Pulse doppler radar

Tracking Radar: Tracking with radar, Monopulse tracking, Conical scan and sequential lobing, Tracking in range, Target acquisition

Other types of Radar: UWB Radar, Millimeter Wave Radar, Internet of Radars (IoR)

UNIT – III

Detection of Signals in Noise: Introduction, Matched filter receiver, Correlation detectors, Detection criteria, Detection characteristics

Radar Receivers: Radar receiver, Receiver noise figure, Noise figure of networks in cascade, Effective noise temperature, Mixers, Low noise frontends, Radar displays

UNIT – IV

Introduction to Satellite Communication: Benefits of satellite communication, Historical evolution of communication satellites, Satellite communication in India, Elements of satellite communication, Types of satellites, Satellite services

Satellite Orbits and Orbital Parameters: Types of Orbits, Kepler's laws, Orbital elements, Satellite orbits, Orbital perturbations, Satellite location from an earth station, Satellite launching

UNIT – V

Space Segment: Satellite configuration, Transponder subsystem, Antenna subsystem, AOC sub system, TT&C subsystem, Power and Thermal subsystem

Earth Station Technology: Elements of earth station, Types of earth station, Earth station transmitter, Earth station receiver, Antenna and feed systems, Antenna tracking, High power and low noise amplifiers, Up and down converter, IF equipment, Baseband equipment

Text Books:

1. Merrill I. Skolnik, "Introduction to Radar Systems", 3rd Edition, Tata McGraw Hill, 2017.
2. R. N. Mutagi, "Satellite Communication, Principles and Applications", 1st Edition, Oxford University Press, 2016.

References:

1. Peyton Z. Peebles, "Radar Principles", 2nd Edition, John Wiley, 2007.
2. J.C. Toomay, Paul Hannen, "Principles of Radar", 3rd Edition, PHI, 2010.
3. Dennis Roddy, "Satellite Communications", 4th Edition, McGraw Hill, 2017.

Course Outcomes (COs):

1. Interpret the significance of radar and radar range equation. (POs – 1, 2, 3, 8, 10, 12, PSOs – 1, 3)
2. Apply Doppler principle in the detection of targets and to distinguish between Doppler and tracking radars. (POs – 1, 2, 3, 6, 7, 8, 10, 12, PSOs– 1, 3)
3. Analyze the presence of signals in noise at radar receivers. (POs – 1, 2, 3, 8, 10, 12, PSOs – 1, 3)
4. Understand the characteristics of satellite communication orbits and launching methods. (POs –1, 2, 3, 8, 10, 12, PSOs – 1, 3)
5. Describe the different types of models in designing space segments and earth station technology. (POs – 1, 2, 3, 8, 10, 12, PSOs – 1, 3)

MACHINE AND DEEP LEARNING

Course Code: ECE642 **Credits: 3:0:0**
Prerequisites: Information, Learning and Inference **Contact Hours: 42**
Course Coordinator: S. Sethu Selvi

UNIT – I

Introduction: What is machine learning, Example machine learning applications

Supervised Learning: Learning a class from examples, VC dimension, PAC learning, Noise, Learning multiple classes, Regression, Model selection and generalization

Bayesian Decision Theory: Classification, Losses and Risks, Discriminant functions, Association rules

UNIT – II

Parametric Methods: Maximum likelihood estimation, Evaluating an estimator, Bayes estimator, Parametric classification, Regression, Tuning model capacity

Dimensionality Reduction: Subset Selection, Principal Component Analysis (PCA), SVD and Matrix factorization, Linear Discriminant Analysis (LDA)

UNIT – III

Unsupervised Learning: Clustering: k–Means Clustering, EM algorithm, Hierarchical Clustering, Decision Trees: Univariate and Multivariate trees

UNIT – IV

Multilayer Perceptrons: Perceptron, Training a perceptron, Learning Boolean functions, Multilayer perceptrons, Backpropagation algorithm, Training procedures, Dimensionality reduction, Deep learning

Deep neural networks: Deep feed forward networks, regularization for deep learning

UNIT – V

Deep neural networks: Optimization for training deep models, convolutional networks

Sequence Modeling: Recurrent and Recursive nets, LSTM, Gated RNNs, Practical methodology, Applications

Text Books:

1. Ethem Alpaydin, “Introduction to Machine Learning”, 3rd Edition, PHI Learning Pvt. Ltd, 2015.
2. Ian Goodfellow, Yoshua Bengio, Aaron Courville, “Deep Learning”, MIT Press, 2017.

References:

1. Christopher Bishop, “Pattern Recognition and Machine Learning”, CBS Publishers & Distributors, 2010.
2. Tom Mitchell, “Machine Learning”, McGraw Hill, 1997.
3. Michael Nielsen, “Neural Networks and Deep Learning”, 2019.

Course Outcomes (COs):

1. Examine the concepts of various supervised learning algorithms and employ Bayesian learning for classification (POs – 1, 2, 3, 4, 8, 12, PSO – 3)
2. Evaluate parametric methods for classification and investigate various dimensionality reduction algorithms (POs –1, 2, 3, 4, 8,12 PSO – 3)
3. Analyse unsupervised learning algorithms and multivariate concepts (POs –1, 2, 3,4, 8, 12, PSO – 3)
4. Appreciate the concepts of deep learning and apply deep feed forward network practical problems (POs –1, 2, 3, 4, 5, 8, 12, PSO – 3)
5. Apply convolutional networks and demonstrate functioning of recurrent and recursive neural networks (POs –1, 2, 3, 4, 5, 8, 12, PSO – 3)

SPEECH AND AUDIO PROCESSING

Course Code: ECE643 **Credits: 3:0:0**
Prerequisites: Digital Signal Processing **Contact Hours: 42**
Course Coordinators: K. Indira, Sadashiva V. Chakrasali

UNIT – I

Speech Production and Hearing: Process of speech production, Acoustic theory of speech production, Lossless tube models, Anatomy and physiology of the ear, Sound perception

UNIT – II

Speech Analysis: Short time speech analysis, Time domain parameters, Frequency domain parameters, LPC analysis and Cepstral analysis

UNIT – III

Speech Enhancement and Speech Synthesis: Speech enhancement techniques, Filtering and adaptive noise cancellation, Principles of speech synthesis and synthesizer methods

UNIT – IV

Speech and Speaker Recognition: Basic pattern recognition approach, Parametric representation, Dynamic time warping, Hidden Markov models, Language models, Speaker recognition techniques and features that distinguish speakers

UNIT – V

Audio Processing: Indian musical instruments, features used for classification of instruments, music analysis, audio streaming, audio standards

Text Books:

1. Douglas O' Shaughnessy, "Speech Communications", 2nd Edition, University Press, 2004.
2. Shaila D. Apte, "Speech and Audio Processing", Wiley India Edition, 2012.

References:

1. L. R. Rabiner, R. W. Schafer, "Digital Processing of Speech Signals", Pearson Education, 2016.
2. Thomas F. Quatieri, "Discrete Time Speech Signal Processing", Pearson Education, 2014.

Course Outcomes (COs):

1. Discuss the generation of speech and sound perception (POs – 1, 2, 8, 12, PSO – 3)
2. Analyze speech signals based on time domain and frequency domain features (POs – 1, 2, 3, 4, 8, 12, PSO – 3)
3. Discuss the techniques used in speech enhancement and synthesis (POs – 1, 2, 3, 4, 8, 12, PSO – 3)
4. Recognize the differences between speech recognition and speaker recognition (POs – 1, 2, 3, 4, 6, 8, 12, PSO – 3)
5. Recognize the need of audio processing and appreciate audio coding standards (POs – 1, 2, 3, 8, 12, PSO – 3)

LOW POWER VLSI DESIGN

Course Code: ECE644 **Credits: 3:0:0**
Prerequisites: CMOS VLSI Design **Contact Hours: 42**
Course Coordinator: U S Pavitha

UNIT – I

Power Dissipation in CMOS: Introduction: Need for low power VLSI chips, Sources of power consumption, Introduction to CMOS inverter power dissipation, Low power VLSI design limits, Basic principle of low power design

UNIT – II

Logical Level Power Optimization: Gate reorganization, Local restructuring, Signal gating, Logic encoding, State machine encoding, Pre-computation logic

Circuit Level Power Optimization: Transistor and gate sizing, Equivalent pin ordering, Network restructuring and re-organization, Special latches and flip-flops

UNIT – III

Low Voltage Low Power Adders: Standard adder cells, CMOS adder's architecture, Low voltage low power design techniques, Current mode adders

Special Techniques: Power reduction and clock networks, CMOS floating gate, Low power bus, Delay balancing

UNIT – IV

Low Voltage Low Power Multipliers: Overview of multiplication, Types of multiplier architectures, Braun multiplier, Baugh-Wooley multiplier, Booth multiplier, Wallace tree multiplier, Delay balancing in multipliers

Low Voltage Low Power Random Access Memories: Basics of SRAM and DRAM, Memory cell, Pre-charge and equalization circuit, Types of DRAM, Output latch

UNIT – V

Synthesis for Low Power: Behavioral level transforms, Algorithm level transforms for low power, Architecture driven voltage scaling, Power optimization using operation reduction, Operation substitution, Bus switching activity

Text Books:

1. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 2008.
2. Kiat-Seng Yeo, Kaushik Roy, "Low Voltage Low power VLSI Subsystems", Tata McGraw Hill Publications, 2009.

References:

1. Jan M. Rabaey, Massoud Pedram, “Low Power Design Methodologies”, Kluwer Academic Publishers, 2010.
2. Prof.Ajit Pal, IIT Kharagpur, NPTEL Lecture series on “Low Power Circuits and Systems”, June 2012.
3. P. Chandrakasan, R.W. Broadersen, “Low Power Digital CMOS Design”, Kluwer Academic Publishers, 1995.

Course Outcomes (COs):

1. Apply lowpower design concepts to classify power dissipation mechanisms in CMOS integrated circuits. (POs – 1, 2, 4, 8, 9, 12, PSO – 2)
2. Classify various power optimization techniques at circuit and logic level. (POs –1, 2, 4, 6, 8, 12 PSO – 2)
3. Design low power low voltage adders and special circuits. (POs – 1, 2, 5, 6, 8, 12, PSO – 2)
4. Design lowpower low voltage memory circuits using current generation design style. (POs –1, 2, 4, 5, 8, 11, 12, PSO – 2**)**
5. Analyze different low power transforms and logic synthesis techniques (POs –1, 2, 4, 5, 8, 12 PSO – 2**)**

OPEN ELECTIVES OFFERED FROM THE DEPARTMENT

V – VIII SEMESTER

MICROCONTROLLER AND APPLICATIONS

Course Code: ECOE01 **Credits: 3:0:0**
Prerequisites: Fundamentals of Computing **Contact Hours: 42**
Course Coordinator: Sara Mohan George

Unit I

Overview of Microcomputer systems: Purpose of micro controller, Difference between microprocessor and microcontroller, Block diagram of a microcontroller, Microcontroller functioning, Harward and Von-Neumann Architecture, RISC and CISC processors, Basic memory organization, addresses, interrupts.

Unit II

ARM Processor and fundamentals: Registers, Current Program Status, Pipeline, Exceptions, Interrupts and Vector Table, Architecture Revisions, ARM Architecture families.

Unit III

Internal architecture: Introduction to ARM7TDMI processor – Internal architecture, Overview of Instruction Set and Instruction Cycle timings, ARM 32- bit and THUMB (16-bit) operating modes, Switching between ARM and THUMB instructions. Types of memory – Code memory, External Memory, Internal memory

Unit IV

C Programming for Microcontrollers: Data types: Local Variable Types, Function argument types, Signed and unsigned types, C Looping Structures, Register allocation, Function Calls, Pointer aliasing, Unaligned data and endianness

Unit V

Ports and Interfacing Applications: General purpose input/output ports, Interfacing of ADC, DAC, LCD, stepper motor, LED, keypad and 7-segment display, Development Tools: Simulators, debuggers, cross compilers, in-circuit Emulators for the microcontrollers.

Text Book:

1. Andrew N. Sloss, “ARM system Developers Guide”, Elsevier, 2009.

Reference Book:

1. Douglas V Hall, “Microprocessors and Interfacing”, Tata McGraw-Hill Education, 3rd edition, 2017

Course Outcomes (COs):

At the end of the course the student will be able to

1. Understand the basic concepts of microcontrollers – (POs –1, 2, 8, PSO – 2)
2. Comprehend the fundamentals of ARM processor – (POs –1, 2, 8, PSO – 2)
3. Explain the internal architecture of ARM – (POs –1, 2,8, PSO – 2)
4. Write C code that will compile on ARM Architecture – (POs –1, 2, 5,8, PSO – 2)
5. Design interfacing applications using LPC2148 – (POs –1, 2, 5, 8, 12, PSO – 2)

IMAGE PROCESSING WITH PYTHON

Subject Code: ECOE02 **Credits: 3:0:0**
Prerequisites: Nil **Contact Hours: 42**
Course Coordinator: S Sethu Selvi

UNIT – I

Introduction: Getting started with image processing, image processing pipeline, image input/output, image display, basic image manipulations, image formation – sampling and quantization, convolution

UNIT – II

Image Enhancement: Point-wise intensity transformations, histogram processing, gradient, Laplacian, sharpening, unsharp masking, edge detection

UNIT – III

Image Processing: Morphological binary operations, feature detectors vs descriptors, SIFT, Haar-like features

UNIT – IV

Image Segmentation: Hough transform, thresholding, edge/region based segmentation

UNIT – V

Machine and Deep Learning in Image Processing: Clustering, PCA, Eigen faces, image classification, object detection, image classification with Tensor flow, Popular deep CNNs

Textbooks:

1. Sandipan Dey, "Hands-on Image Processing with Python", Packt Publishing Ltd., 2018.
2. R. C. Gonzalez, R. E. Woods, "Digital Image Processing", 4th Edition, Pearson Publishers, 2018.

References:

1. R. C. Gonzalez, R. E. Woods, S. L. Eddins, "Digital Image Processing using MATLAB", 3rd Edition, Gatesmark Publishing, 2020.

Course Outcomes (COs):

1. Appreciate the image processing pipeline and basic image manipulations (POs – 1, 2, 3, 4, 5, PSO – 3)
2. Employ point operations and spatial filtering algorithms for image enhancement (POs – 1, 2, 3, 4, 5, PSO – 3)
3. Evaluate various feature detectors and descriptors for image processing (POs – 1, 2, 3, 4, 5, PSO – 3)
4. Describe image segmentation algorithms using edges and regions (POs – 1, 2, 3, 4, 5, PSO – 3)
5. Examine machine and deep learning algorithms for image classification and object detection (POs – 1, 2, 3, 4, 5, PSO – 3)

FUNDAMENTALS OF NEURAL NETWORKS

Subject Code: ECOE03 **Credits: 3:0:0**
Prerequisites: Nil **Contact Hours: 42**
Course Coordinator: Maya V Karki

UNIT – I

Introduction to Artificial Neurons, Neural Network and Architecture: Fundamental Concepts and Models of Artificial Neural Systems, Biological Neurons and their artificial models, Architectures: feed forward and feed backward. ANN terminologies. Salient properties of Neural networks. Evolution of Neural networks. Applications of ANN.

UNIT – II

Geometry of Binary Threshold Neurons and Their Networks: Pattern recognition and data classification. Basic models of artificial neural network McCulloch-Pitts, Linear separability, Non linearity separability problems, Neural Learning: Supervised and Unsupervised Learning. Neural Network Learning Rules – Hebbian Learning Rule and implementation

UNIT – III

Supervised Learning Network: Perceptron Networks and learning algorithm-Learning and Memory, error corrections and gradient Descent rules. Perceptron learning algorithms and implementation. Single and layer perceptron and Multilayer perceptron. Examples on pattern classification and implementation. Applications of LMS to Noise cancellation.

UNIT – IV

Multilayer Feed forward Networks: Feed forward Recall and Error Back-Propagation Training – Feed forward Recall, Error Back-Propagation Training, Training Errors and Multilayer Feed forward Networks as Universal Approximators (Excluding Examples). Learning Factors – Initial Weights, Cumulative Weight Adjustment versus Incremental Updating. Applications of feedforward networks with implementation.

UNIT – V

Adaptive linear network architecture, training and testing algorithm. Unsupervised Learning Network: Learning objectives, Adaptive resonance network: Fundamental architecture, operating principal and algorithm.

Text Books:

1 S. N. Sivanandam and S.N. Deepa, "Principles of Soft Computing", 2nd Edition, Wiley India Pvt. Ltd.-2014.

1. Satish Kumar: Neural Networks A Classroom Approach– McGraw Hill Education (India) Pvt. Ltd, Second Edition, 2013.

References:

1. S. Rajasekaran, G. A. Vijayalakshmi Pai, "Neural Networks, Fuzzy Logic and Genetic Algorithms: Synthesis and Applications" PHI learning Pvt. Ltd. Second Edition 2017.
2. J.M. Zurada: Introduction to Artificial Neural Systems-J.M. Zurada, Jaico Publications 1994

Course Outcome (COs):

1. Understand the importance of ANN and application domains in computational intelligence. (POs- 1,2, PSO-1)
2. Employ basic concepts of artificial neural network and its architecture (POs- 1, 2, 3, PSO-1)
3. Describe different learning rules and natural processing (POs - 1, 2, 3, PSO-1)
4. Apply single layer perceptron for pattern classification (POs- 1, 2, 3, 4, 5, PSO-1)
5. Analyze pattern classification with multilayer feed forward network (POs- 1, 2, 3, 4, 5, PSO-1)

SENSOR ELECTRONICS

Subject Code: ECOE04 **Credits: 3:0:0**
Prerequisites: NIL **Contact Hours: 42**
Course Coordinator: M Nagabushanam

UNIT – I

Displacement Transducers and Motion Sensors: Basic definitions, Sensing methods, capacitive, Inductive, Potentiometric transducers, Strain gauge, Vibrating wire, Electro-optical, sonar sensors, Application.

Tachometers and Velocity Transducers: Basic definitions, Electromagnetic linear velocity, other linear, Toothed-rotor, other angular speed transducers, Application.

UNIT – II

Gyro and other Attitude Sensors: Basic definitions, Inertial, Gravity, Magnetic, Optical, Radio, flow stream- reference sensing.
Strain gages: Basic definitions, Sensing methods, metal-wire, metal-foil, Deposited metal, Semiconductor strain, Special application gages, Application.

UNIT – III

Humidity and Moisture Sensors: Basic definitions, sensing methods, hygrometric, psychrometric, dew-Point, Remote moisture-sensing methods, Hygrometers, Psychrometers, Dew-point sensors, Condenser, Piezoelectric microphones, Application.

Liquid Level Sensors: Basic definitions, Sensing methods, Float, Conductivity, Capacitive, Heat mass transfer, Photo electric, Vibrating, Ultrasonic, Nucleonic level sensors, Applications.

UNIT– IV

Pressure Transducers and Sound Measuring Microphones: Basic definitions, Sensing methods, Capacitive, Inductive, Reluctive, Potentiometric, Resistive, Strain gage, Piezo electric, Vibration element transducers, Application.
Vacuum sensors: Basic definitions, Sensing methods, Capacitive, Pirani, Thermocouple, Hot cathode, Cold cathode gages, Application

UNIT– V

Thermometers: Basic definitions, Sensing methods, Thermocouple, Thermistor, Diode, Capacitive, Acoustical thermometers, Application.
Optical Detectors: Basic definitions, Sensing methods, Photovoltaic, Photo conductive, Photo emissive, Photo Electromagnetic, Thermoelectric, Bolometer, Pyro electric detectors, Applications.

Text Books:

1. Harry N. Norton “Hand book of Transducers”, 1st Edition, Prentice Hall International, 1989.
2. D. Patranabis, “Sensors and Transducers”, 2nd Edition, PHI Learning Pvt Ltd., 2013

References:

1. E. O. Doebline, “Measurement systems Application and Design”, 4th Edition, Tata, McGraw-Hill, 2007
2. B. C. Nakra and K.K. Choudhury, “Instrumentation Measurement and Analysis”, 2nd Edition, Tata McGraw-Hill Education, 2003

Course Outcomes (COs):

1. Identify various mechanical sensors and its measurement principles (POs-1, 2, 4, PSO-1)
2. Illustrate the fundamental concepts of different sensors and gages (POs-1, 2, 4, PSO-1)
3. Compare the construction and working of various sensors for Industrial Applications (POs-1, 2, 4, PSO-1)
4. Select suitable sensor for the given industrial Applications. (POs-1, 2, 4, PSO-1)
5. Demonstrate the working of sensors used to measure thermal and optical variables. (POs-1, 2, 4, PSO-1)

AUTOMOTIVE ELECTRONICS

Subject Code: ECOE05 **Credits: 3:0:0**
Prerequisites: Nil **Contact Hours: 42**
Course Coordinator: Roshan Zameer Ahmed

UNIT – I

Automotive Fundamentals Overview: Ignition System, Spark plug, Spark pulse generation, Ignition Timing, Brakes, Steering System, Battery, Starting System.

UNIT – II

Sensors: Oxygen (O2/EGO) Sensors, Throttle Position Sensor (TPS), Engine Crankshaft Angular Position (CKP) Sensor, Magnetic Reluctance Position Sensor, Engine Speed Sensor, Ignition Timing Sensor, Hall effect Position Sensor, Knock Sensor, Optical Crankshaft, Manifold Absolute Pressure (MAP) Sensor

UNIT – III

Actuators: Fuel Metering Actuator, Fuel Injector, Ignition Actuator

Exhaust After-Treatment Systems: Catalytic Converter, Exhaust Gas Recirculation (EGR), Evaporative Emission Systems, electronic engine control systems and electronic ignition control systems

UNIT – IV

Vehicle Motion Control: Antilock Brake System (ABS), Electronic Steering Control, Power Steering, Traction Control, Electronically controlled suspension.
Integrated Body: Safety Systems.

UNIT – V

Automotive Diagnostics: Timing Light, Engine Analyzer, On-board diagnostics, Off-board diagnostics, Expert Systems.

Future Automotive Electronic Systems: Alternative Fuel Engines, Collision Avoidance Radar warning Systems, Low tire pressure warning system, Radio navigation.

Text Books:

1. William B. Ribbens**, "**Understanding Automotive Electronics", 8th Edition, SAMS/Elsevier Publishing, 2017.

References:

1. Robert Bosch GmbH, "Automotive Electrics Automotive Electronics Systems and Components", 5th edition, John Wiley& Sons Ltd., 2007.

Course Outcomes (COs):

1. Explain fundamentals of automotive electronics systems for different applications. (POs - 1, 2, 5, PSO - 2)
2. Apply the knowledge of embedded systems in terms of sensor functioning to build subsystems for automotive electronics. (POs - 1, 2, 5, PSO - 2)
3. Analyze the functioning of actuator systems involved in the exhaust after-treatment system, engine control system and ignition control system using electronics. (POs - 1, 2, 5, PSO - 2)
4. Apply the knowledge of electronics in vehicle motion control systems, antilock braking systems, steering control systems suspension systems and communication system using electronics. (POs - 1, 2, 5, PSO - 2)
5. Identify defects in engine operation using automotive diagnostics and future automotive electronic systems. (POs - 1, 2, 5, PSO -2)

EMBEDDED AND INTERNET OF THINGS

Subject Code: ECOE06 **Credits: 3:0:0**
Prerequisites: Nil **Contact Hours: 42**
Course Coordinator: K V Suma

UNIT – I

Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, communication interfaces.

UNIT – II

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages
Characteristics and Quality Attributes of Embedded Systems

UNIT – III

Embedded system design and development: System design and development, life-cycle models- the waterfall model, the V cycle model, the spiral model and rapid prototyping incremental, problem solving – five steps to design
Introduction & Concepts: Definition and Characteristics of IoT, Things in IoT, IoT Protocols, IoT Functional Blocks, IoT Communication Models

UNIT – IV

Developing Internet of Things: IoT Platform design methodology - Specifications: Requirements, Process, Domain, Information, Services, IoT Level, Functional View, Operational View, Device & Component Integration and Application Development
IoT Systems – Logical Design using Python: Data Types and Data Structures, Control Flow, Functions, Modules, Packages, File Handling, Date and Time Operations, Classes

UNIT – V

IoT Case Studies: Home Automation: Smart Lighting, Home Intrusion Detection; Cities: Smart Parking Environment: Weather Monitoring System, Weather Reporting Bot, Air Pollution Monitoring, Forest Fire Detection; Agriculture – Smart Irrigation, IoT Printer.

Text Books:

1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 1st edition, reprint 2014.
2. Arshdeep Bahga, Vijay Madisetti, "Internet of Things: A Hands-on Approach", University Press, 2015.

References:

1. James K Peckol, "Embedded Systems – A Contemporary Design Tool", John Wiley, 2nd Edition 2008.

Course Outcomes (COs):

1. Identify the basic building blocks of embedded systems (POs – 1, 2, 8, PSO -2).
2. Comprehend the characteristics and quality attributes of embedded systems (POs – 1, 2,8, PSO -2).
3. Analyze the complete life cycle of embedded system design and development with basics of IoT. (POs – 1, 2, 3, 5, 8, 12, PSO -2).
4. Learn basics of design, integration and applications of IoT models. (POs-1, 2, 8, PSO -2)
5. Appraise with various case studies. (POs-1, 2, 8, PSO -2)